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DELIVERABLE D60.4

1k x 1k pnCCD Conceptual Design

WP60 Advanced Instrumentation Development

1ST Reporting Period

November 2014

PROJECT GENERAL INFORMATION

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Project's coordinator: Dr. Manuel Collados Vera, IAC.

Tel: (34) 922 60 52 00

Fax: (34) 922 60 52 10

E-mail: mcv@iac.es

Project website address: http://solarnet-east.eu/

SOLARNET
Reporting period 2013-04-01 - 2014-09-30

Author: Alex Feller (MPG)
Work package: WP 60 “Advanced Instrumentation Development”, subWP 4 “Fast Imaging Polarimeter”
Participants: MPG, PNSensor, IRSOL, KIS

Work carried out during the reporting period

FSP I

An FSP evaluation model (Feller et al. 2014), based on a small pnCCD sensor (cf. Table 1), has been developed to assess the actual performance of the novel polarimeter concept. An initial pnCCD was procured from PNSensor (PNS) in 2012 and has been extensively tested in the lab, where it has performed according to specifications.

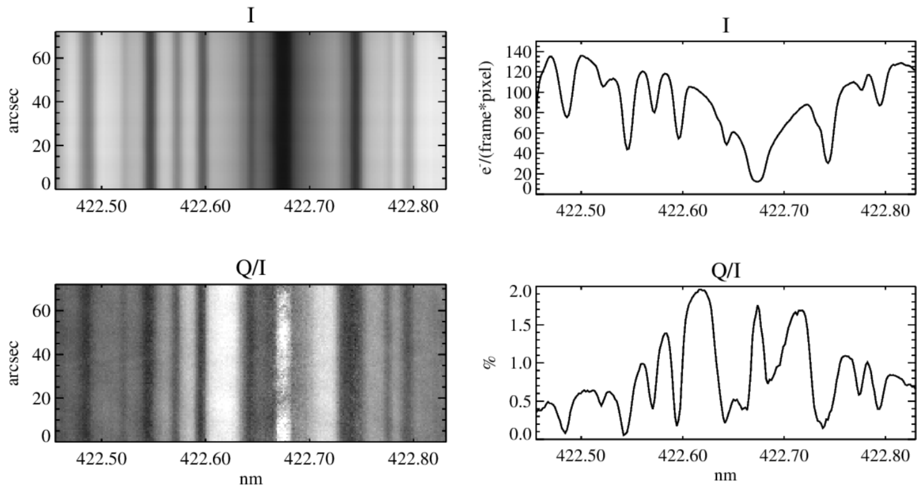

Fig. 1: Scattering polarization in the solar Ca I 422.7 nm spectral line, close to the solar limb. Observed with FSP I at the VTT spectrograph during the June 2013 test campaign.

In a final evaluation step, 3 test campaigns at the VTT solar telescope on Tenerife have been carried out in June and November 2013, and June 2014 (with the first 2 campaigns technically supported by PNS), FSP I has been operated at the VTT spectrograph and at the TESOS Fabry-Pérot filtergraph, thus representing the two standard types of solar post-focus instrumentation. The VTT campaigns have allowed us assess the polarimetric performance under realistic observing conditions which cannot be simulated in the lab. The invaluable practical experience at the telescope, and the data analysis have allowed us to further constrain the sensor and camera requirements for the second development phase (FSP II).

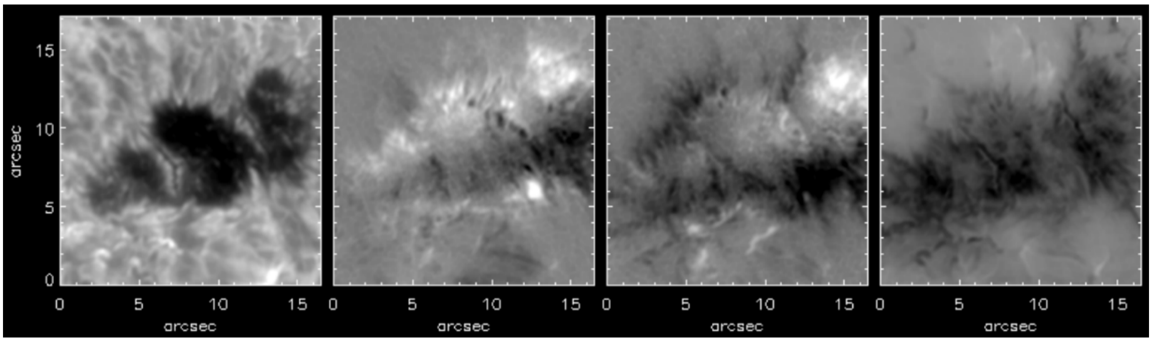

Fig. 2: Snapshot of a times series of a small active region (pore), recorded in the blue wing of the Fe I 630.2 nm spectral line. From left to right: Stokes I (intensity), Stokes Q and U (linear polarization) and Stokes V (circular polarization). Observed with FSP I during the VTT/TESOS filtergraph test campaign in June 2014.

FSP II - design and manufacturing of a 1k x 1k pnCCD camera

Two parallel and competitive conceptual design studies have been carried out by PNS and by the semiconductor lab of the Max Planck society (german: Halbleiterlabor, HLL). Both studies have been based on an advancement of the established pnCCD technology (e.g. Hartmann et al. 2008 and references therein) following different technical approaches and strategies. After a careful balancing of technical and financial arguments we have finally decided to dismiss the PNS study, and to proceed with the further FSP II development in collaboration with HLL.

The HLL conceptual sensor study has addressed the following main issues (also partly described in the PNS report) and has come up with design solutions that are in full compliance with our science requirements:

- Reduction of pixel pitch from 48 μm to 36 μm
- Re-design of PHI bus in order to cope with the required frame transfer time (~100 μs), the smaller pixel pitch, and the larger number of pixels compared to FSP I, yielding higher peak currents into the PHI registers
- Optimization of the common-mode correction method to avoid light-insensitive sensor columns in the imaging area
- Testing of the VERITAS-1 readout ASIC to check compliance with noise requirements

- Re-design of the sensor based readout structures (JFET staggering, Fig. 3) to comply with the smaller pixel pitch

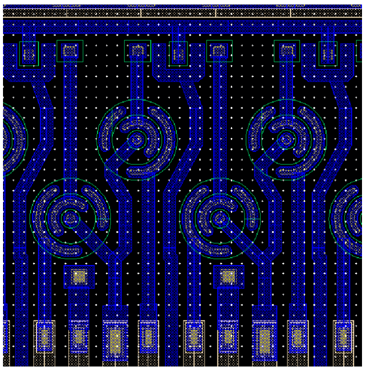

Fig. 3: Layout of sensor readout area with staggered JFETS adapted to the 36 µm pixel pitch and structures for row-wise charge reset.

- Sufficient thermal decoupling of the the VERITAS ASICs from the sensor

- Optimization of the entrance window coating to the blue part of the visible spectrum (Fig. 4). The new coating design will be tested on photodiodes in November 2014, prior to the coating of the science-grade sensor.

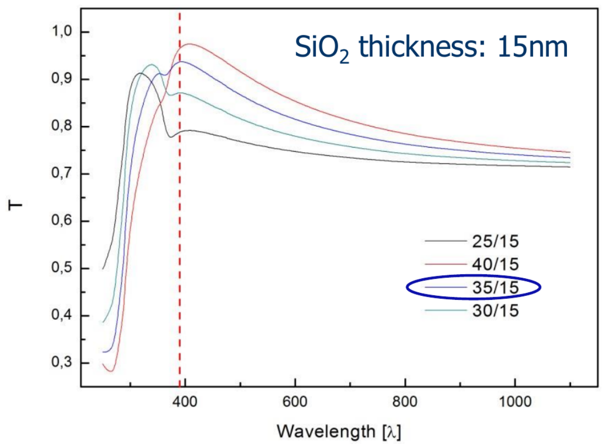

Fig. 4: Sensor quantum efficiency (QE) as a function of different Si_3N_4 [nm] / SiO_2 [nm] coating layer thicknesses. For the FSP II sensor the thickness combination 35/15 nm has been chosen, which yields an increased sensitivity in the blue region of the visible spectrum.

The conceptual study has been followed up by a detailed sensor design which has successfully undergone its design review in April 2014. Sensor manufacturing has started in June 2014 and is expected to be completed in March 2015. Table 1 summarizes the main differences in the specifications between the FSP I and FSP II sensors.

In parallel to sensor design and manufacturing, HLL and MPG are studying all other aspects of the FSP II camera. In the following paragraphs we shortly sketch those activities.

Mechanical mounting and sensor cooling

The sensor, which covers a total area of 40 mm x 80 mm, needs to cooled down to temperatures around -30°C. The temperature distribution across the sensor must not exceed certain limits and has to be extremely stable in time to allow for precise calibration.

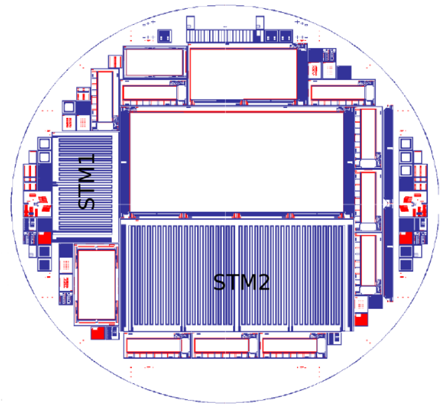

Fig. 5: Diagrams of the test wafer carrying structural and thermal sensor models (STMs) with heater pads

HLL has manufactured structural and thermal sensor models (STMs, Fig. 5) to verify the mechanical mounting concept and the sensor cooling. The tests will be carried out in a TV chamber prior to the assembly of the science-grade sensor.

System layout

The systems layout concept includes readout, power, control electronics and analog-digital conversion, as well as data transfer and data acquisition.

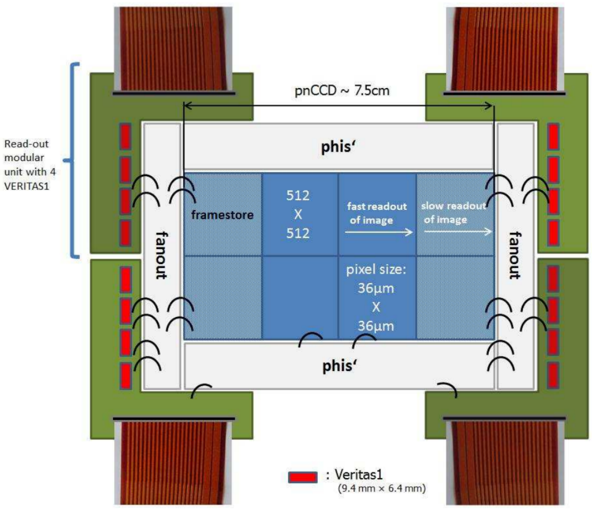

Fig. 6: Conceptual layout of the focal plane array (FPA). See text for a more detailed description.

The photon charges accumulated in the light-sensitive 1k x 1k sensor area are transferred within about 120 µs to 2 adjacent 512 x 1024 frame store areas where they undergo a columnwise readout by 16 VERITAS-1 ASICS during the exposure of the next frame. These fast split-transfer and integrate-while-read concepts allow for frame rates up to 400 fps and 95% duty cycle, which are two of the most crucial camera specifications derived directly from the science application. The VERITAS-1 ASICS have a demonstrated noise figure of about 4 e^- rms at 4.5 µs cycle time (Porro et al. 2013), which is another essential specification for our science.

The amplified signals are multiplexed to 16 x 2 ASIC analogue outputs, channeled through dedicated PCB vacuum feeds and then fed to external ADCs. The ADC, sequencer and other camera related electronics will be mounted on standardized Igel-light PCB boards and accommodated in an external rack next to the camera. The 16-bit data are transferred via 1Gb/10 Gb ethernet connections to a data acquisition (DAQ) computer which is able to deal with the challenging data rate of 6.7 Gb/s, and data volumes of about 6 TB/day which are expected during a typical observing campaign.

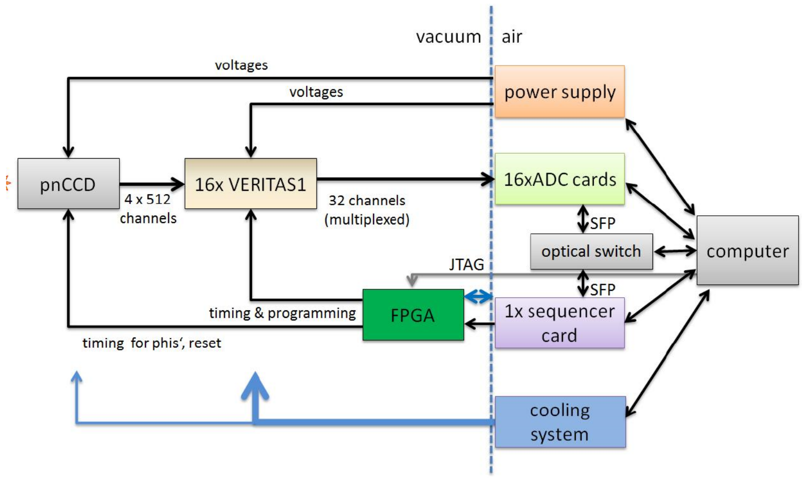

Fig. 7: Conceptual FSP II system layout incl. camera electronics and DAQ system.

Camera housing

The sensor will be mounted in a vacuum enclosing to avoid condensation, and to allow for stable cooling conditions. The housing is completed by an electronics compartment under normal pressure including power, housekeeping and analogue data connections. The detailed design of the camera housing will be completed by the end of 2014, and manufacturing is scheduled for Q1/2015.

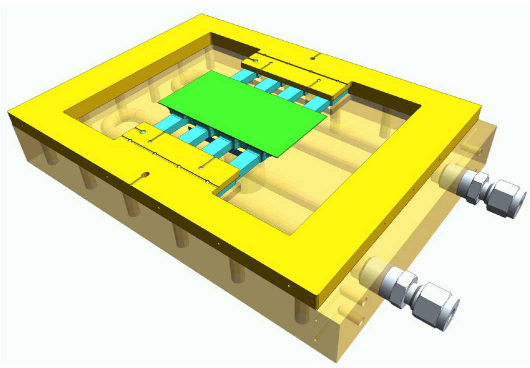

Fig. 8: Part of the sensor vacuum enclosing showing the sensor (green) in the center, the polysilicon cooling block (blue) for heat distribution, the FPA frame (yellow) which will later support the quadrant PCBs with the readout ASICS, and the backbone (brown) of the vacuum enclosing with copper tubes for fluid cooling.

Table 1: Basic differences between the specifications of the FSP I and the newly developed FSP II pnCCD sensors and readout electronics

Specification	**FSP I**	**FSP II**
Sensor size	264 px x 264 px	1024 px x 1024 px
Max. frame rate	800 fps	400 fps
Pixel pitch	48 µm	36 µm
Quantum efficiency > 90%	500 nm - 870 nm	350 nm - 500 nm
Frame transfer time / min. duty cycle	50 µs / 95%	120 µs / 95%
Readout ASICS - type x number	CAMEX x 4	VERITAS-1 x 16
Number of ADCs x Bit depth	8 x 14 bit	32 x 16 bit
Max. data rate	0.78 Gb/s	6.7 Gb/s

Use of SOLARNET resources

Statement on deliverable D60.4 and PNS

The PNS conceptual sensor study related to deliverable D60.4 has been covered entirely by SOLARNET funding, which has been allocated to PNS directly as an independent partner. In addition some PNS resources have been used to support our 2 VTT observing campaigns in 2013. In contrast the HLL sensor study and all FSP II related HLL activities within this reporting period have been covered by MPG internal funds.

The deliverable D60.4 is considered complete. In fact the current state of sensor development is already at a much more advanced stage, as described in the previous section.

Within this reporting period, the SOLARNET personnel resources allocated to MPG in terms of this subWP have been invested in the design of the camera housing and sensor cooling. The MPG SOLARNET funds have covered the position of one mechanical engineer for 7 months (2014-03-01 - 2014-09-30).
This position has now been extended with the remaining SOLARNET funding. Future work related to this subWP will address the remaining design work and manufacturing supervision of the FSP II camera housing, and the dual-beam polarization modulator (D60.5, D60.6). We also note here that this position is shared with subWP 3 “Microlens-fed spectrograph”.

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Hartmann et al. 2008, Proc. SPIE 7015, 70155C
Porro et al. 2013, IEEE Transactions on nuclear science, 60, 446